In the Claims

1. (currently amended) A receive circuit comprising:

a data input terminal to receive a stream of input data;

a first sampler having a first sampler data terminal coupled to the data input terminal, a first clock terminal, and a first data output terminal;

a second sampler having a second sampler data terminal coupled to the data input terminal, a second clock terminal and a second data output terminal;

a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node; and

a multiplexer having a first multiplexer input terminal coupled to the first data output terminal, a second multiplexer input terminal connected to the second data output terminal, a select terminal, and a multiplexer output terminal;

wherein the comparison circuit issues an error signal in response to mismatches between the first and second sampled-data streams.

2. (original) The receive circuit of claim 1, wherein the data input terminal, the first sampler, the second sampler, and the comparison circuit are disposed on a semiconductor chip.

3. (original) The receive circuit of claim 1, wherein the first and second samplers sample the stream of input data to produce respective first and second sampled-data streams, and wherein the comparison circuit is adapted to compare at least one of the sampled-data streams with expected data.

4. (canceled)

5. (currently amended) The receive circuit of claim [[4]] 1, wherein the comparison circuit issues an error signal in response to each mismatch between the first and second sampled-data streams.

6. (currently amended) ~~The receive circuit of claim 1, further comprising~~ A receive circuit comprising:

a data input terminal to receive a stream of input data;

a first sampler having a first sampler data terminal coupled to the data input terminal, a first clock terminal, and a first data output terminal;

a second sampler having a second sampler data terminal coupled to the data input terminal, a second clock terminal and a second data output terminal;

a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node;

a multiplexer having a first multiplexer input terminal coupled to the first data output terminal, a second multiplexer input terminal connected to the second data output terminal, a select terminal, and a multiplexer output terminal; and

clock control circuitry coupled to the second clock terminal and to provide the second clock signal, wherein the clock control circuitry is adapted to vary the phase of the second clock signal in response to a timing control signal.

7. (original) The receive circuit of claim 6, wherein the clock control circuitry varies the phase of the first clock signal in response to a second timing control signal.

8. (original) The receive circuit of claim 1, further comprising a third sampler having a third sampler data terminal coupled to the data input terminal, a third clock terminal, and a third data output terminal.

9. (canceled)

10. (previously presented) The receive circuit of claim 1, wherein the first multiplexer input terminal is coupled to the first data output terminal via the comparison circuit.

11. (currently amended) ~~The receive circuit of claim 1,~~ A receive circuit comprising:

a data input terminal to receive a stream of input data;

a first sampler having a first sampler data terminal coupled to the data input terminal, a first clock terminal, and a first data output terminal;

a second sampler having a second sampler data terminal coupled to the data input terminal, a second clock terminal and a second data output terminal;

a comparison circuit having a first comparison-circuit input node coupled to the first data output terminal, a second comparison-circuit input node coupled to the second data output terminal, and a comparison-circuit output node; and

a multiplexer having a first multiplexer input terminal coupled to the first data output terminal, a second multiplexer input terminal connected to the second data output terminal, a select terminal, and a multiplexer output terminal;

wherein the first comparison circuit input node is coupled to the multiplexer output terminal and the first multiplexer input terminal is coupled to the first data output terminal.

12-50 (canceled)

51. (New) The receive circuit of claim 1, wherein the first sampler includes a first reference terminal to receive a first reference voltage and the second sampler includes a second reference terminal to receive a second reference voltage distinct from the first reference voltage.

52. (New) The receive circuit of claim 51, wherein the first and second reference voltages are independently adjustable.

53. (New) The receive circuit of claim 3, wherein the first sampler samples the input data using a first clock signal having a first clock phase and the second sampler samples the input data using a second clock signal having a second clock phase.

54. (New) The receive circuit of claim 53, wherein the first and second clock phases are independently adjustable.

55. (New) The receive circuit of claim 6, wherein the first sampler includes a first reference terminal to receive a first reference voltage and the second sampler includes a second reference terminal to receive a second reference voltage distinct from the first reference voltage.

56. (New) The receive circuit of claim 55, wherein the first and second reference voltages are independently adjustable.